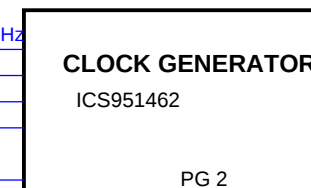
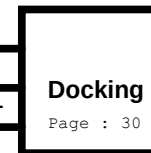
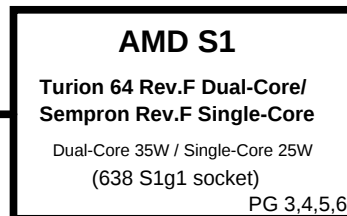
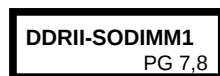
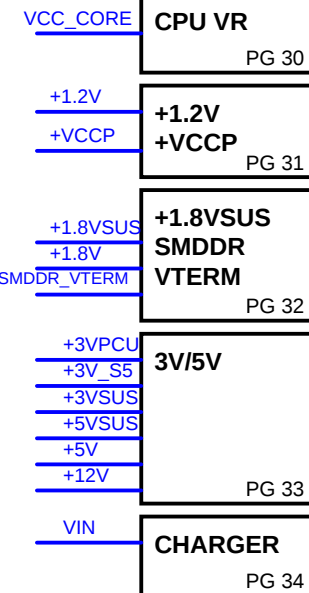


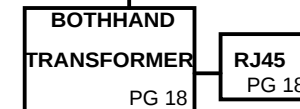
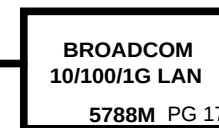
BOM MARK
SA@ SATA 要打
PA@ PATA 要打
3@ 36 要打

ZH3

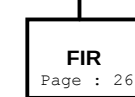
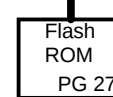
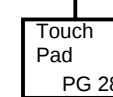
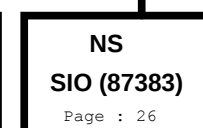
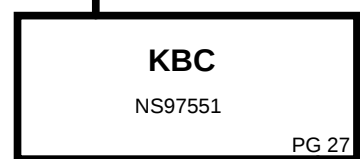
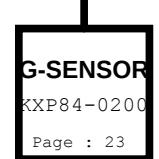
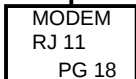
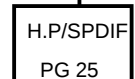
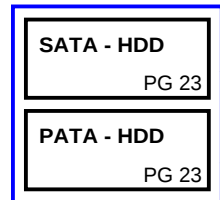
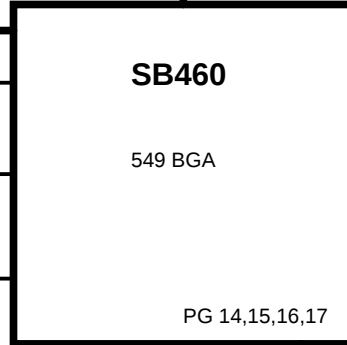
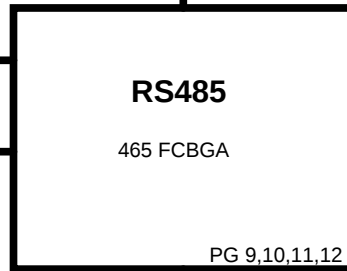
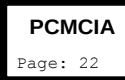
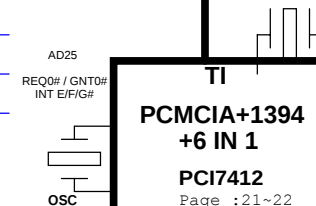
ZH3 ASSY P/N :31ZH3MB0008
ZH3 MB C/S ASSY P/N: 41ZH3CS0001
ZH3 MB S/S ASSY P/N: 51ZH3SS0003

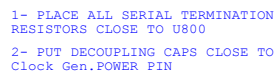
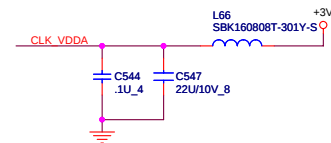


HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
REF 14MHz



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ0# / GNT0#	INT E/F/G#
5788M	AD20	REQ2# / GNT2#	INT G#

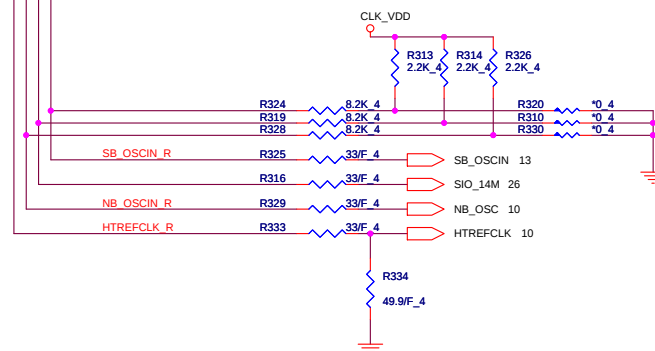
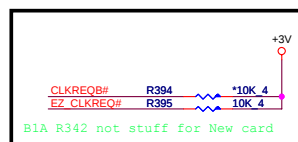




FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

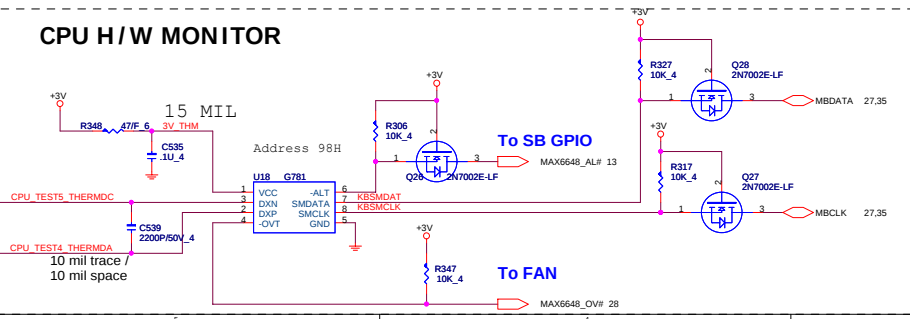
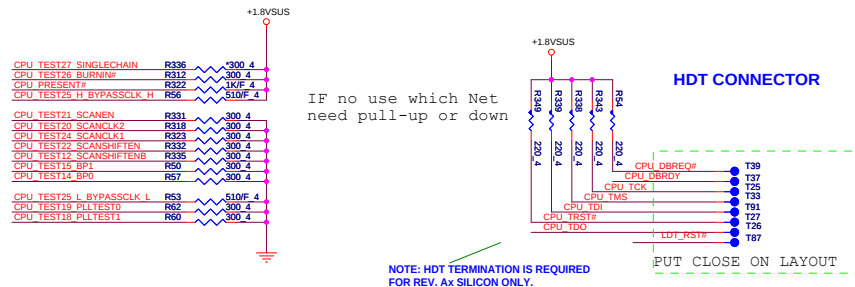
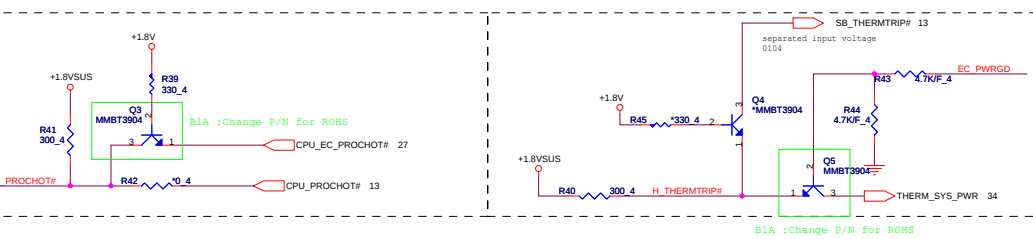
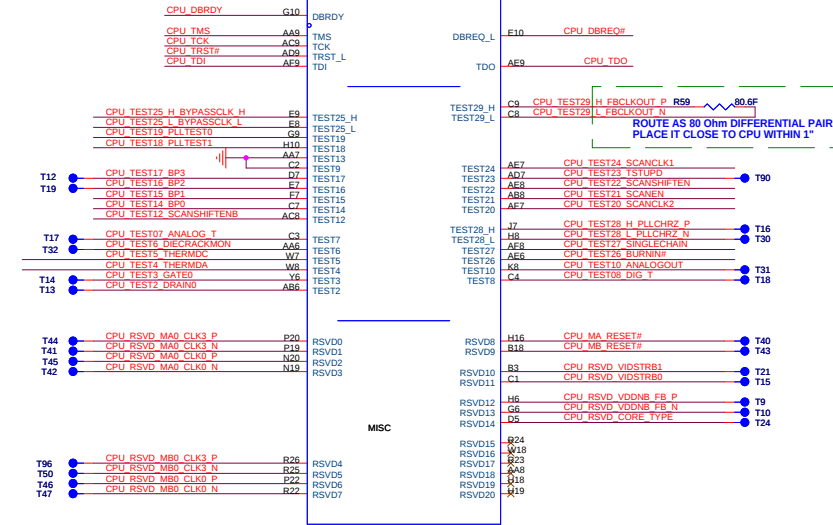
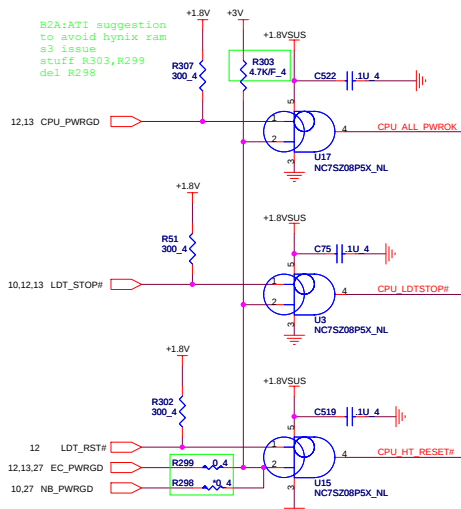
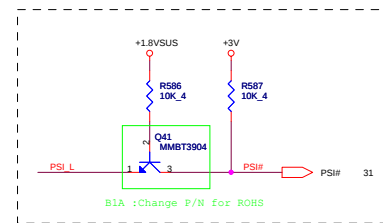
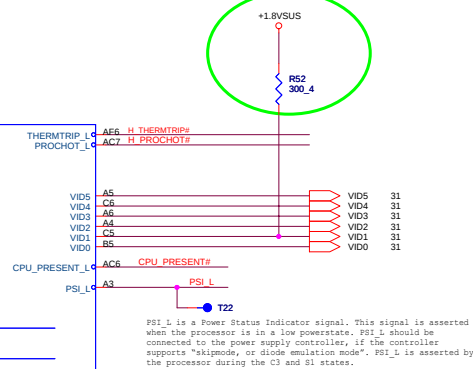
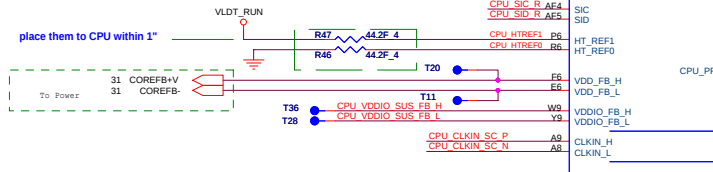
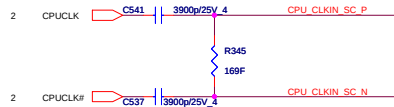
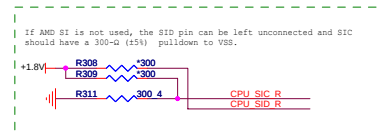
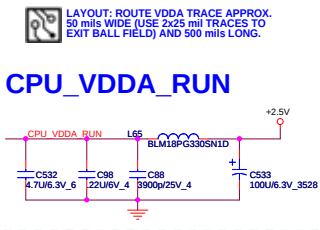
Check AMD clock

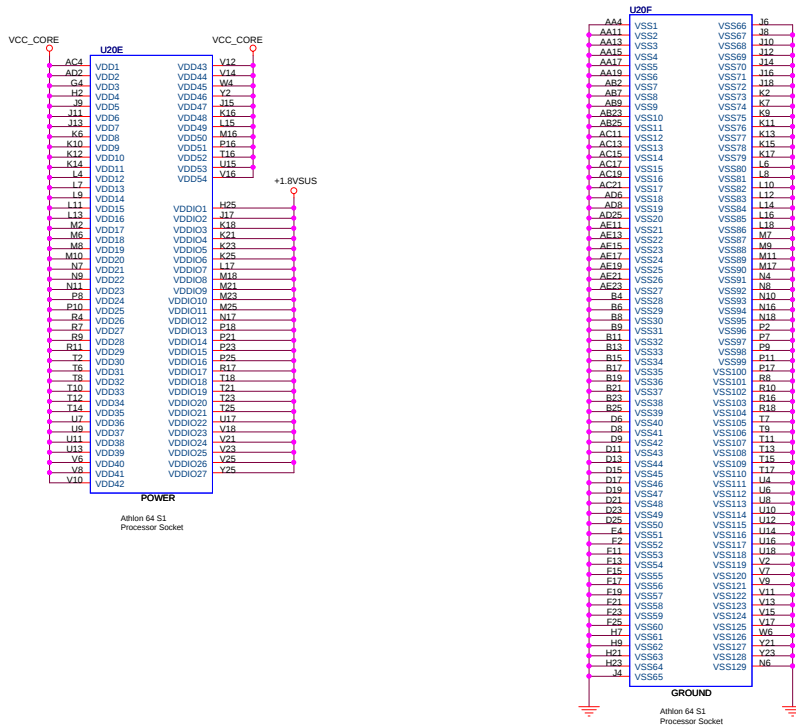
```
CLKREQA# Controls SRC5,6,7
CLKREQB# Controls SRC2,3,4,ATIG3
CLKREQC# Controls SRC0,1,ATIG0,1,2
```



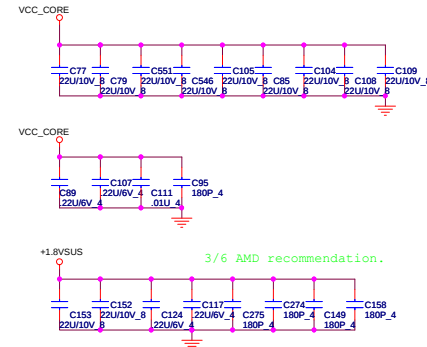


ATHLON Control and Debug

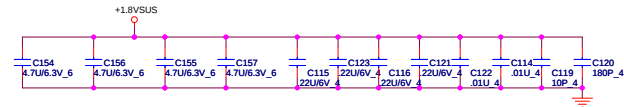




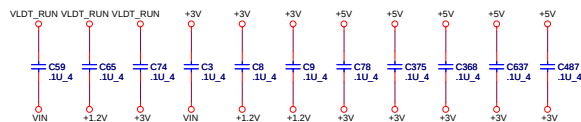
BOTTOMSIDE DECOUPLING



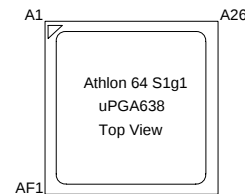
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



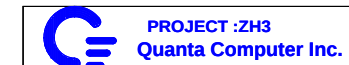
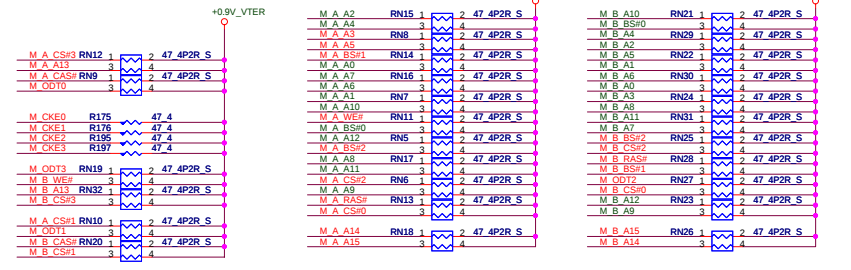
PROCESSOR POWER AND GROUND

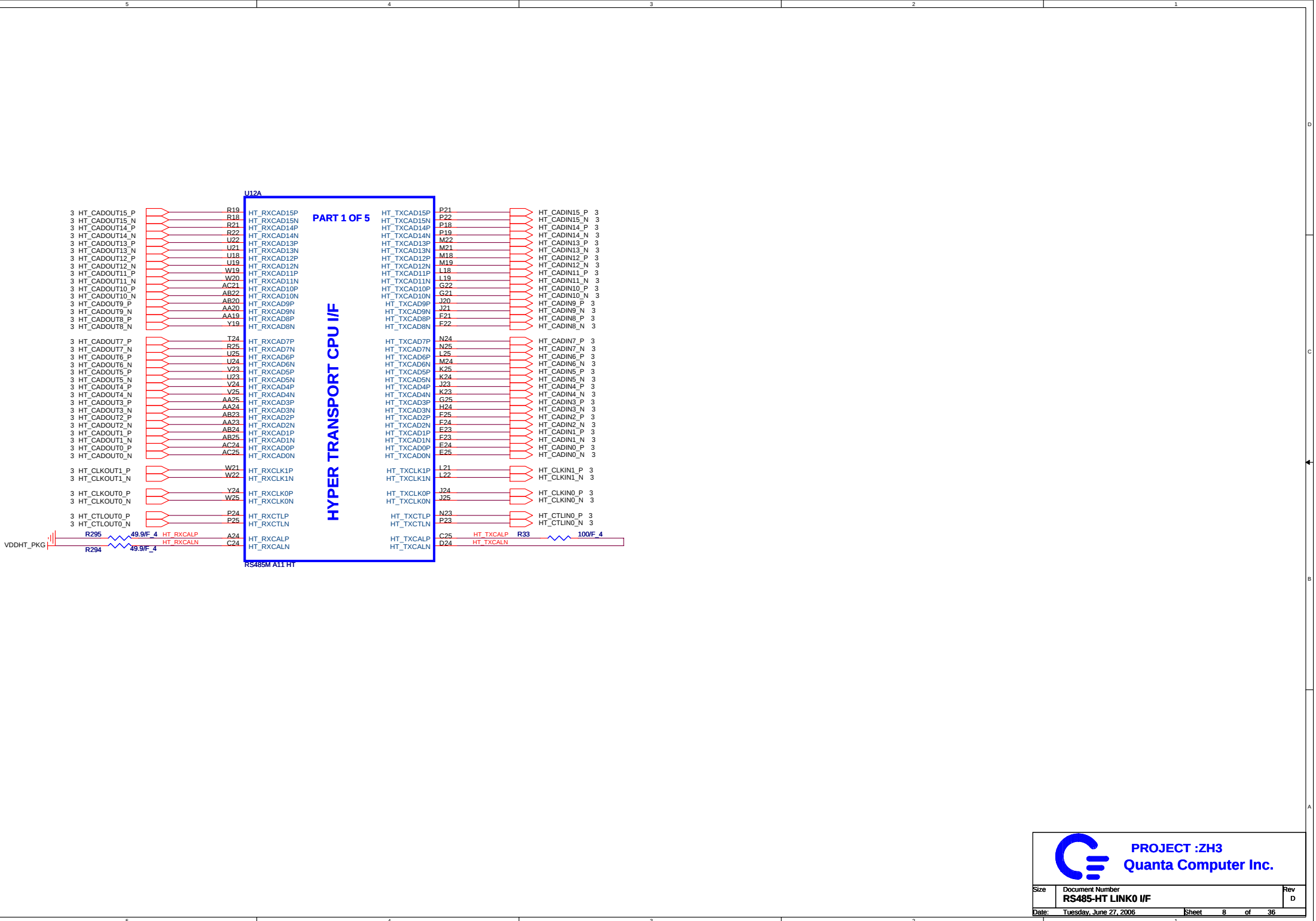


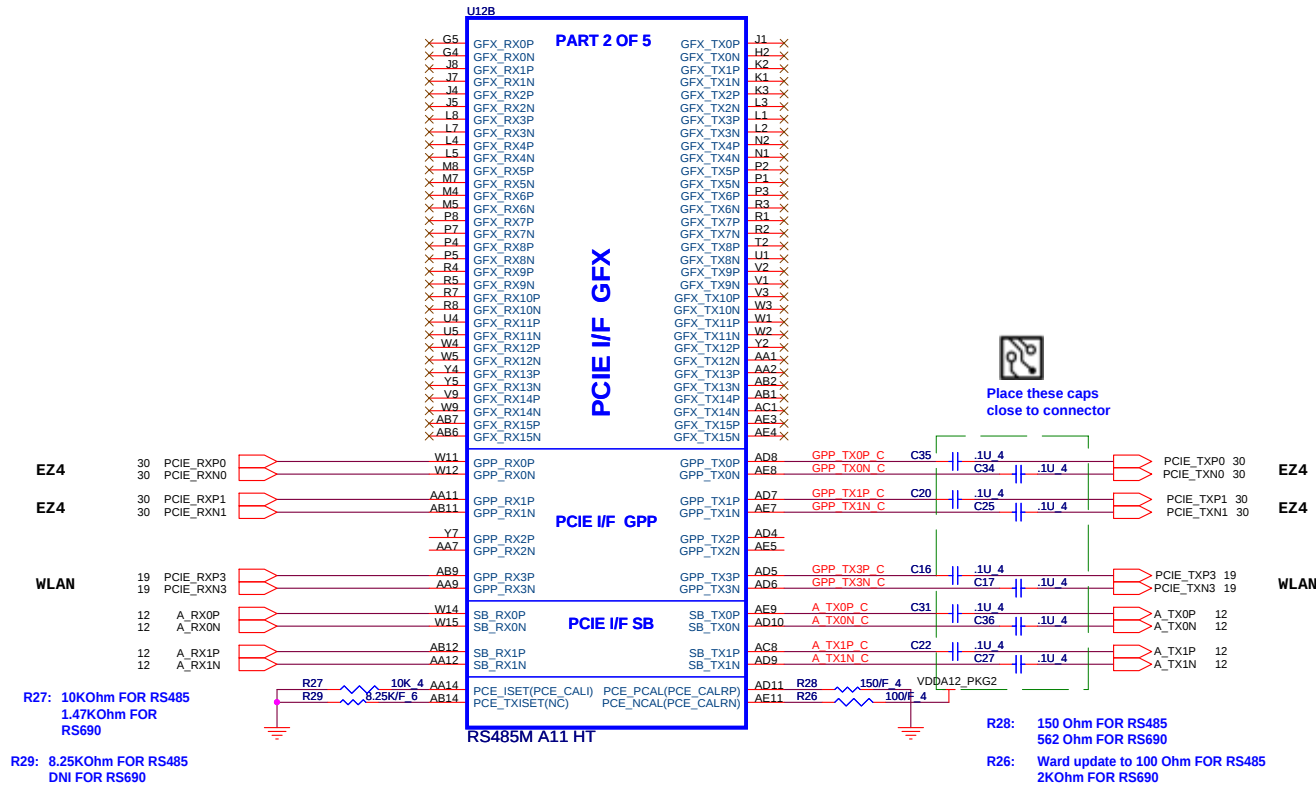
3/6 :ADD 0.1u CAPACITOR TO CROSS POWER PLANE.

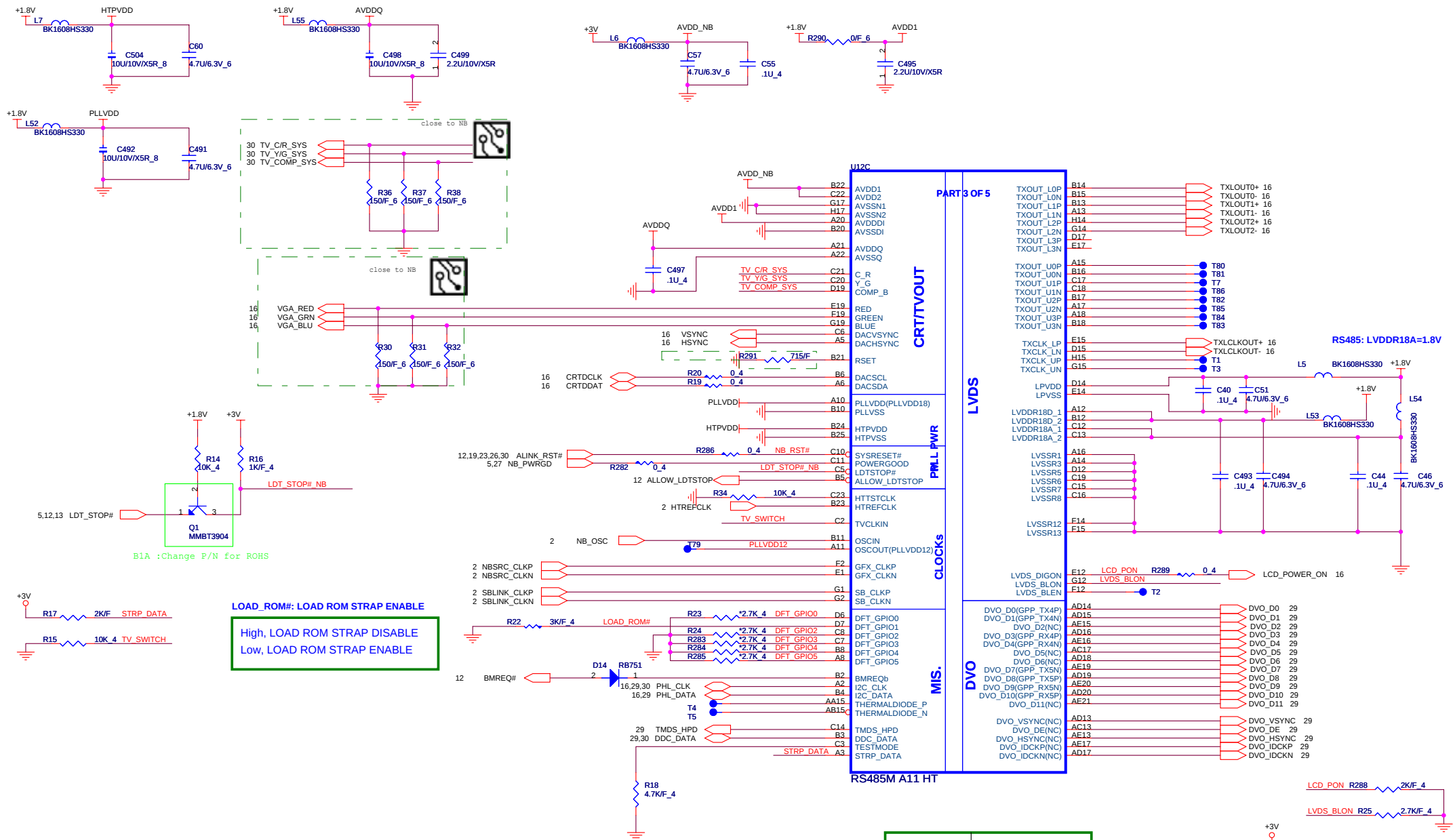


DDR2 TERMINATOR

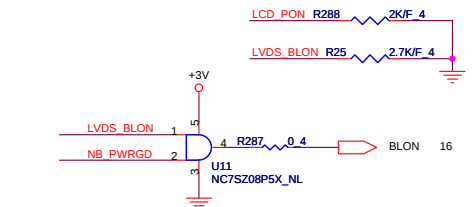




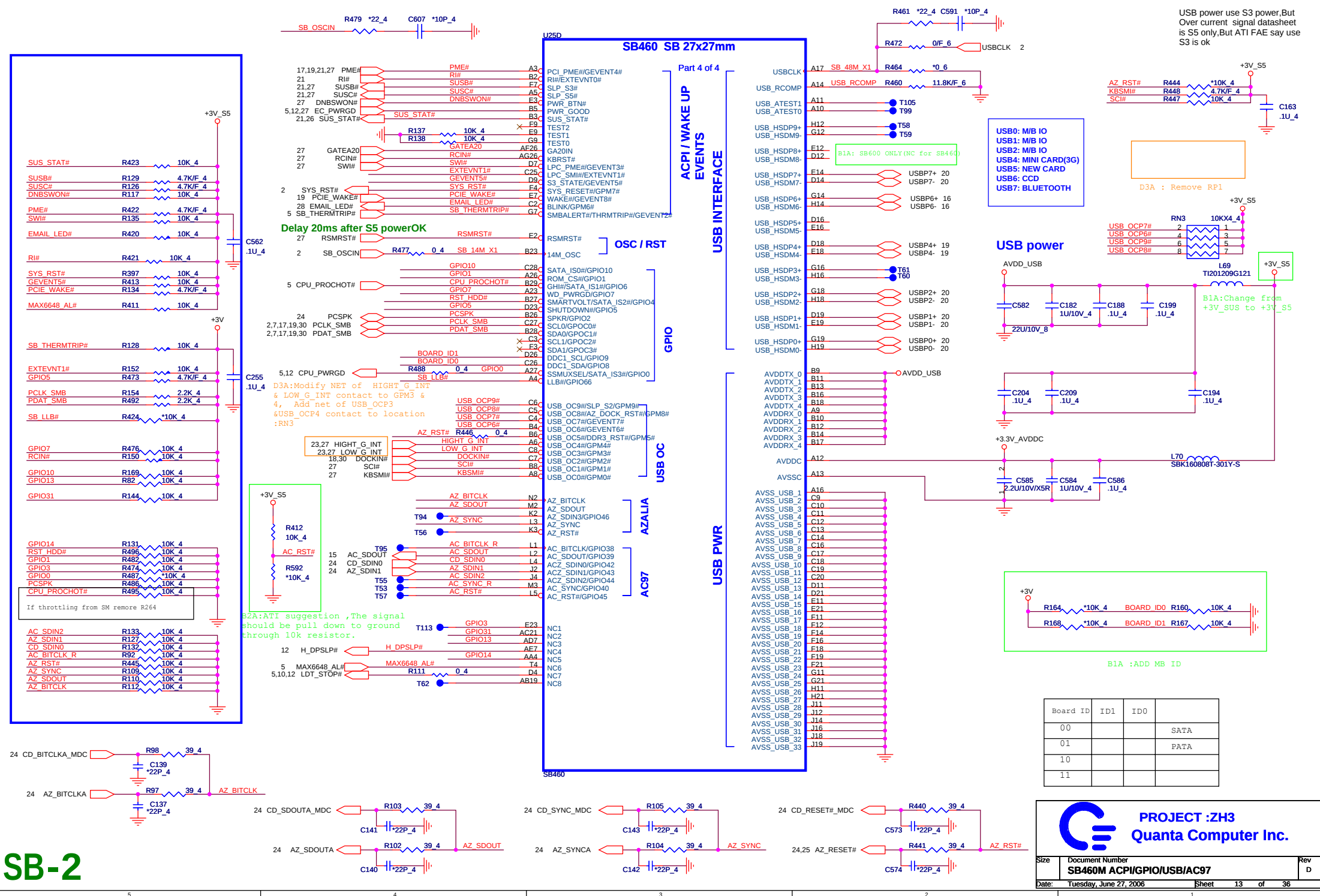


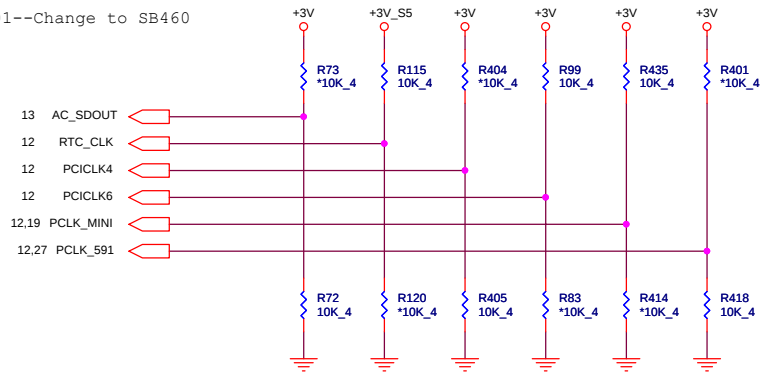


	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P



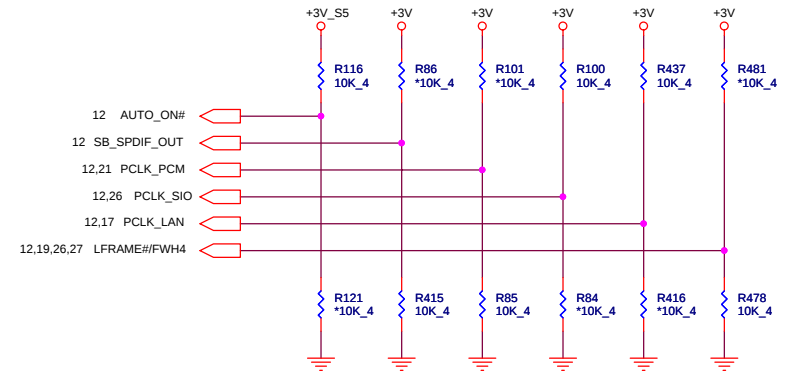
SB-2



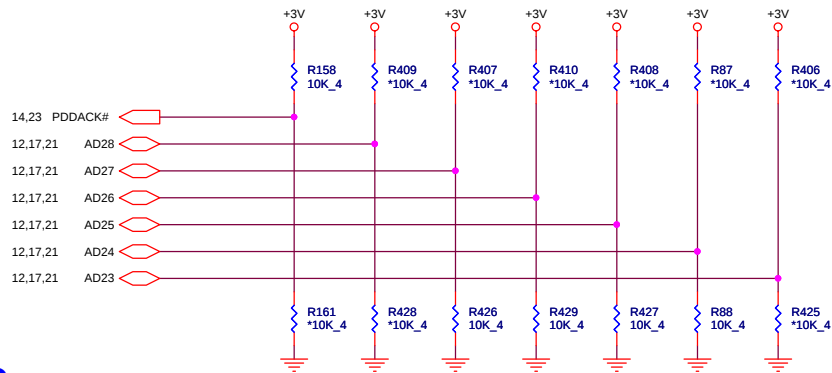


REQUIRED STRAPS

				PCLK_MINI PCLK_591	
PULL HIGH	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	L, L = FWH ROM NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

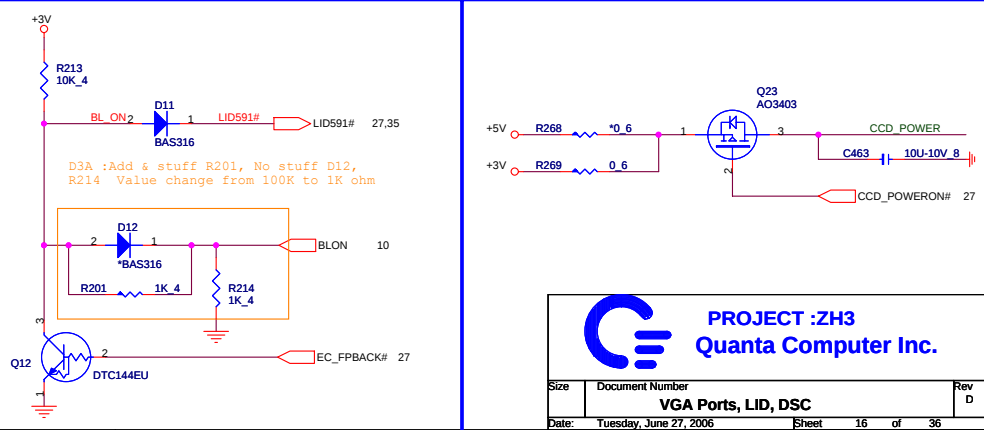
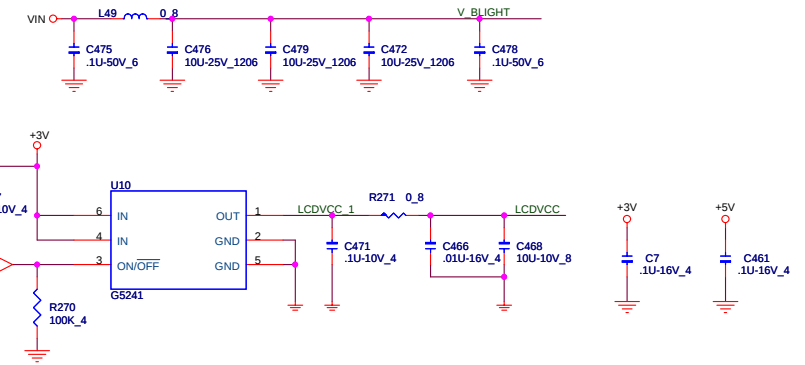


		AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
PULL HIGH	ACPWRON	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	DEFAULT	SIO 48MHz	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH BIOS ENABLE AFTER STARTUP	DISABLE THERMTRIP#



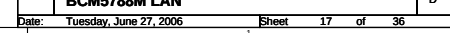
DEBUG STRAPS

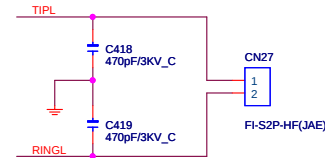
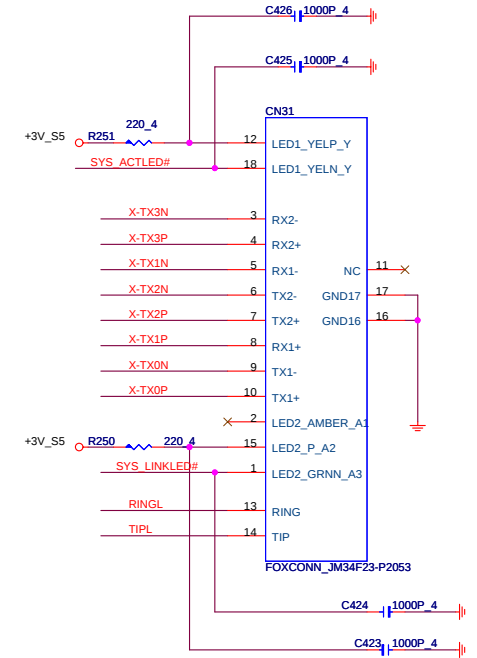
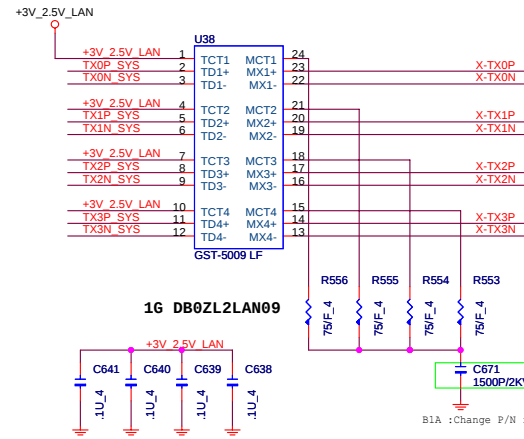
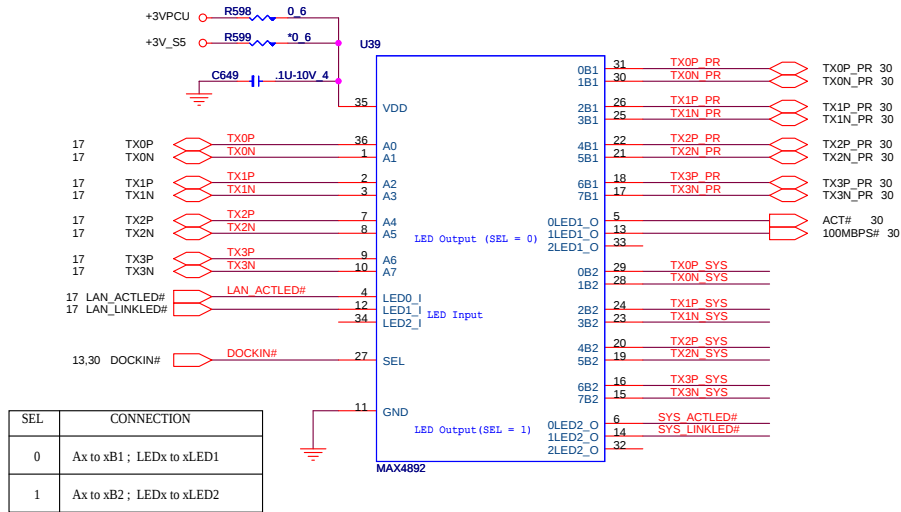
	PDAK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	



PROJECT :ZH3
Quanta Computer Inc.

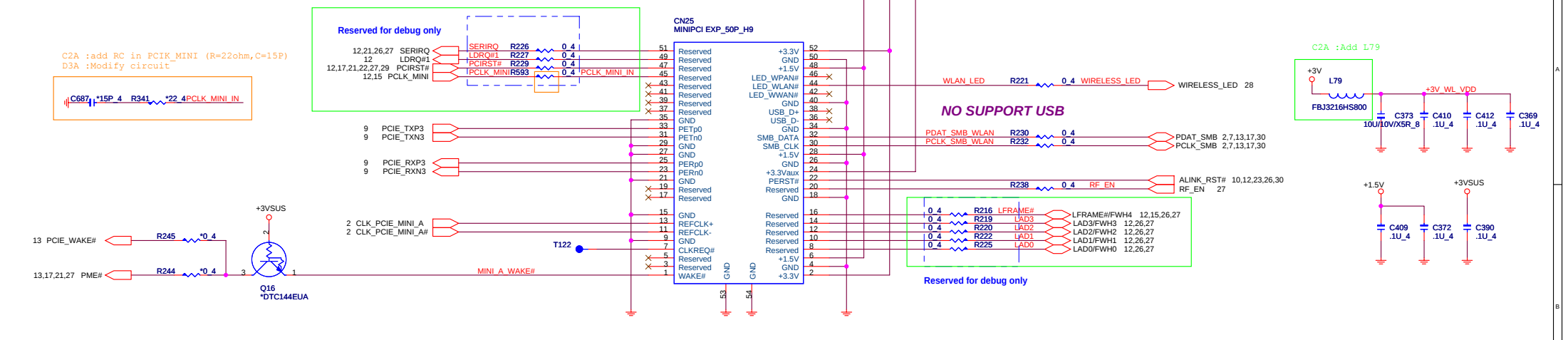
Size	Document Number	Rev D
VGA Ports, LID, DSC		
Date:	Tuesday, June 27, 2006	Sheet 16 of 36



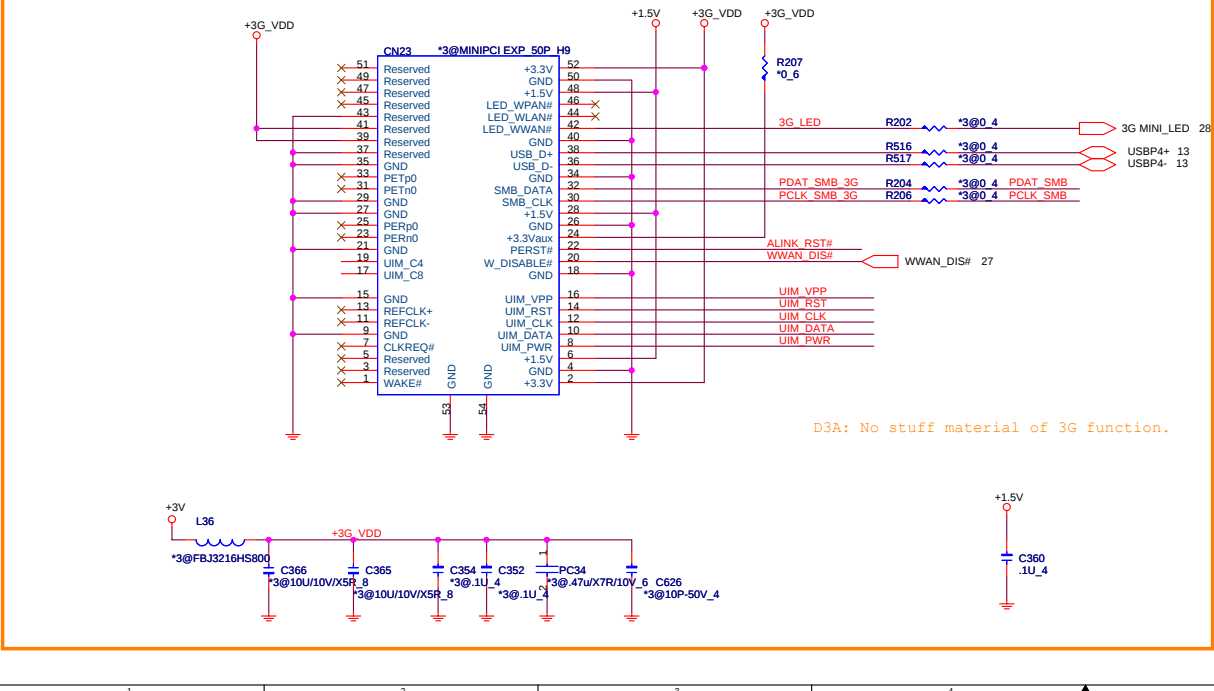


WLAN MINI CARD

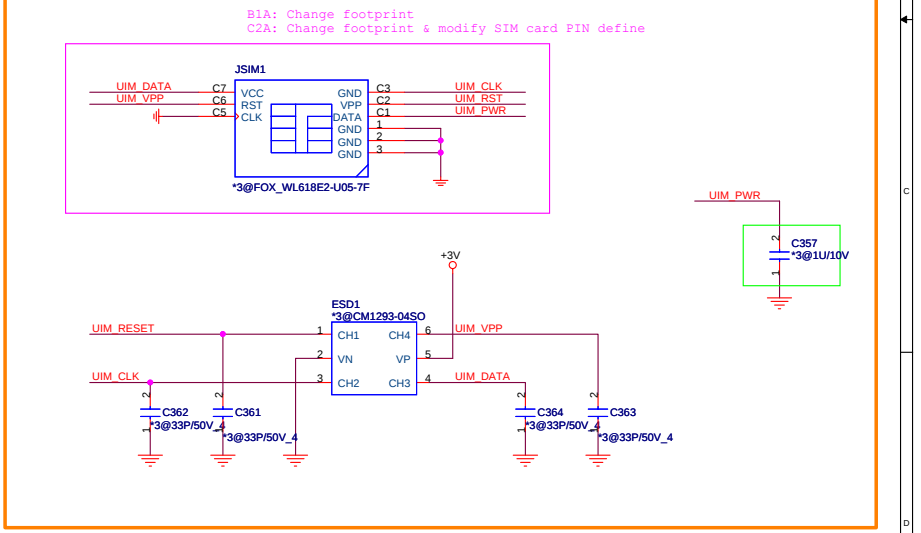
B1A:These signals of reserve have be used by wireless module of Foxconn BG. These signals impact LPC. I remove signal line in order to solve the WLAN issue.



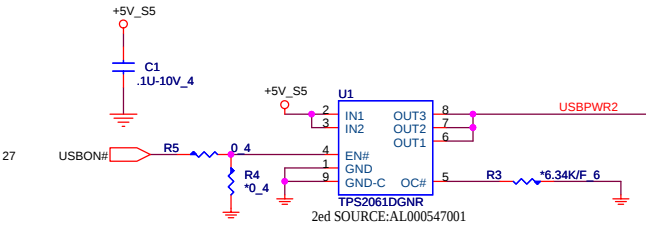
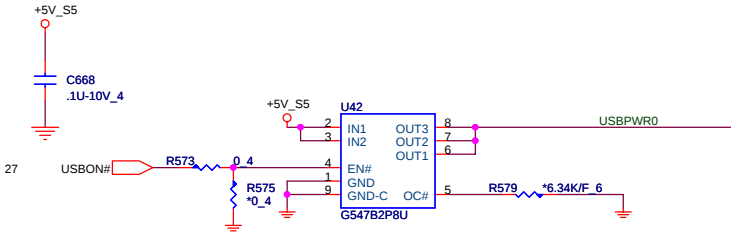
3G MINI CARD



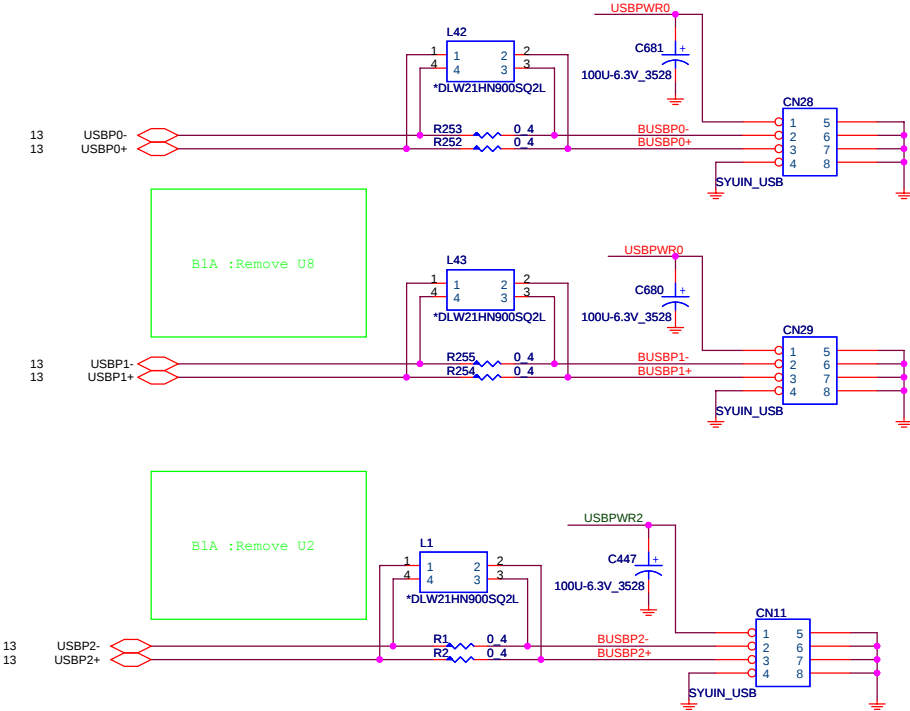
SIM CARD



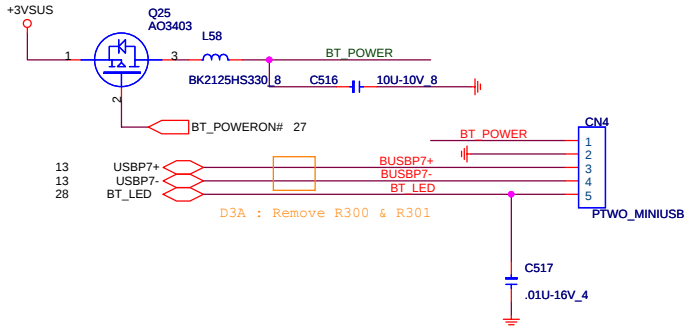
USB POWER SUPPLY

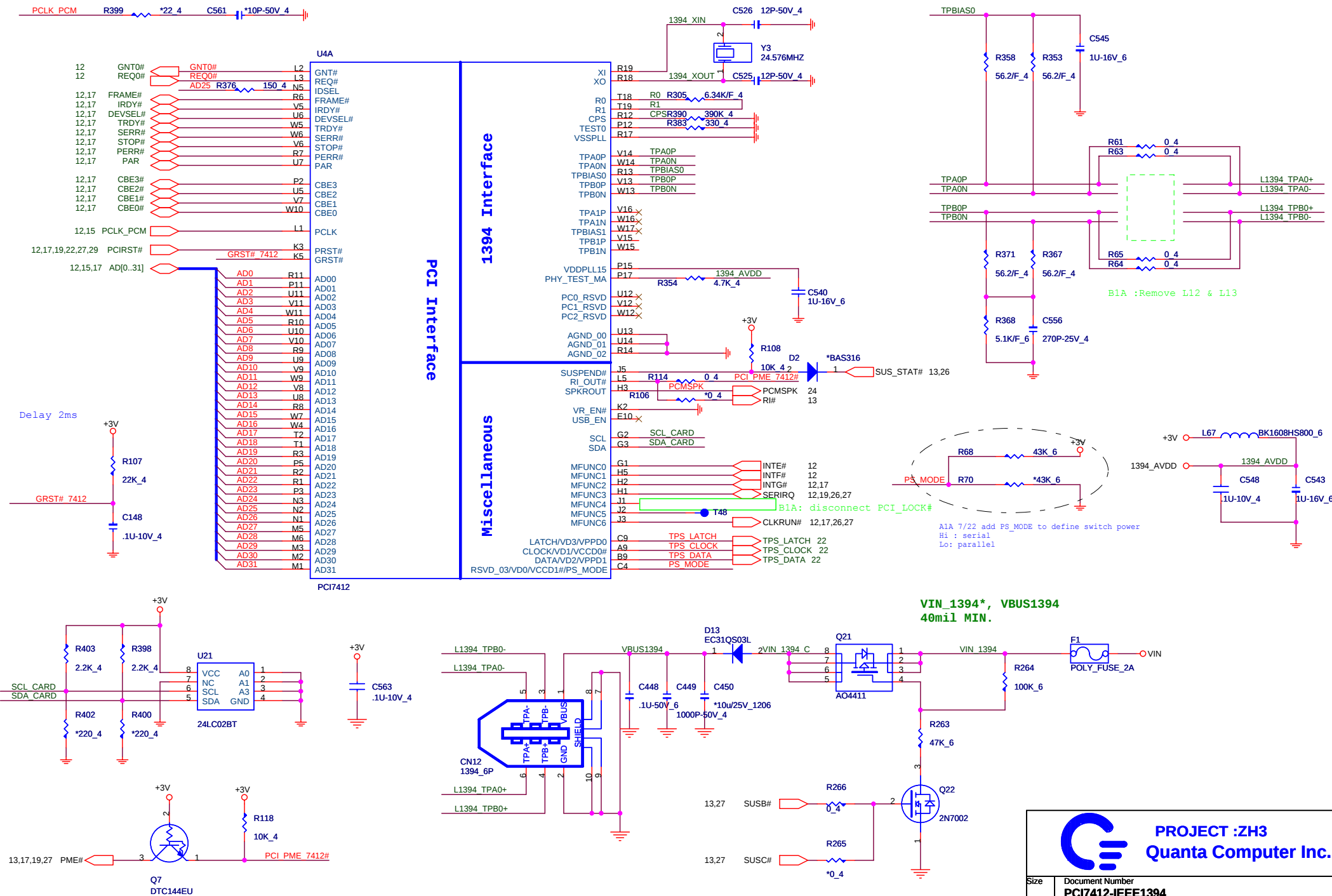


USB



BLUETOOTH MODULE CONNECTOR

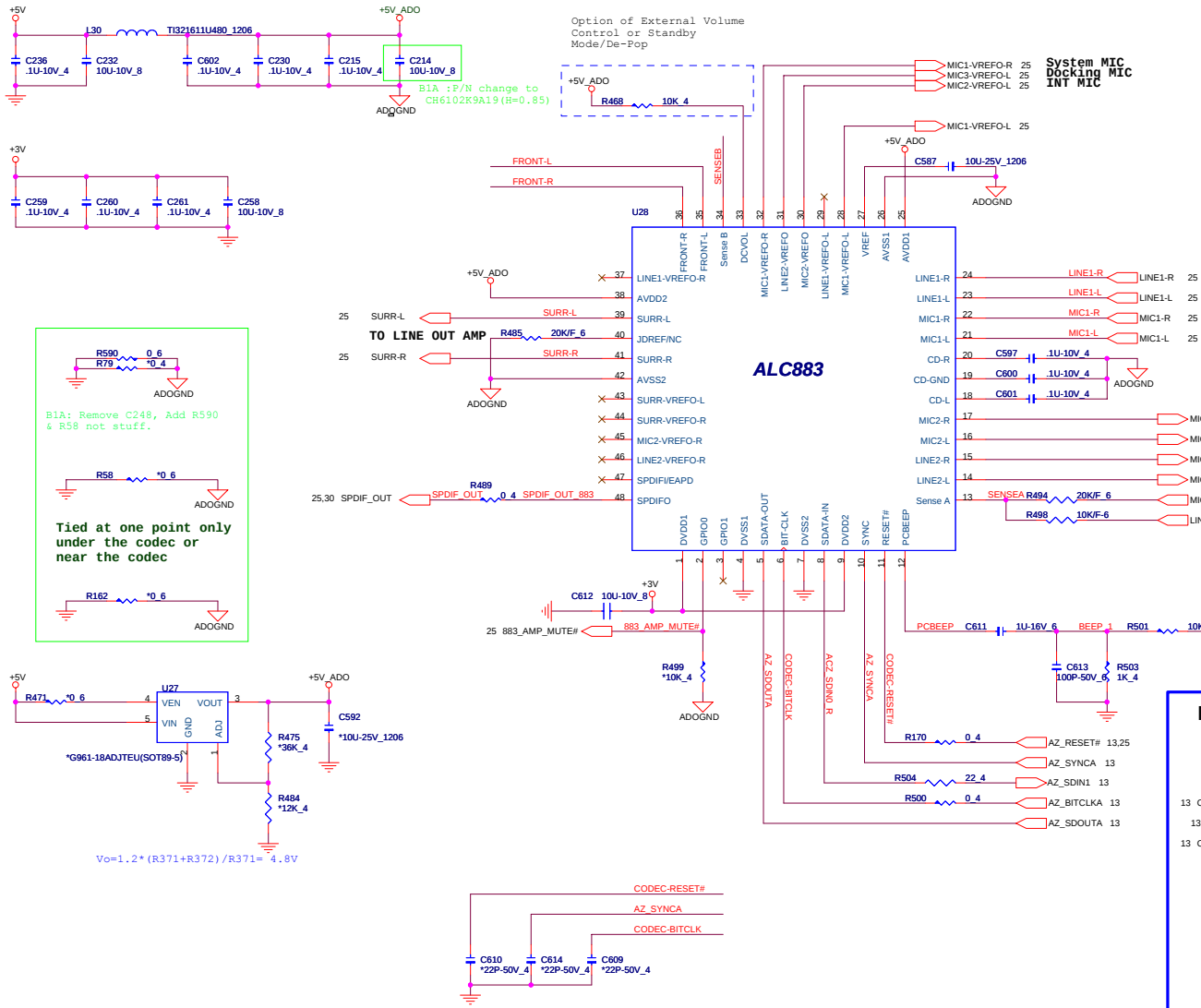




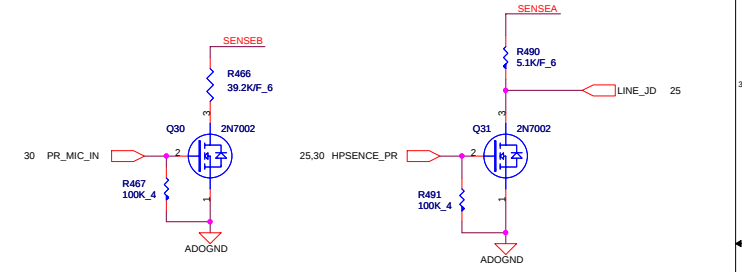
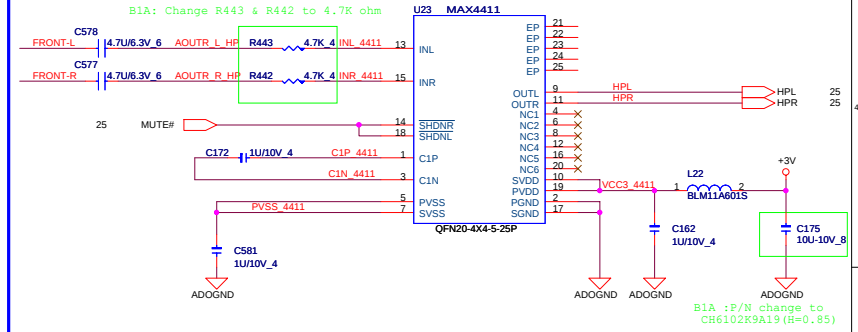
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-IEEE1394	D
Date:	Tuesday, June 27, 2006	Sheet 21 of 36

CODEC (ALC883)

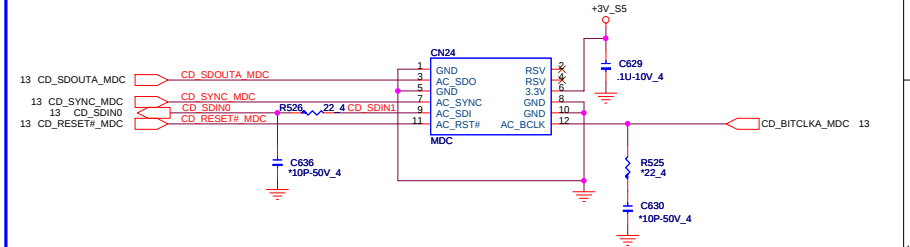


LINE OUT Amplifier



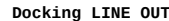
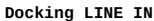
MDC

For MDC Module

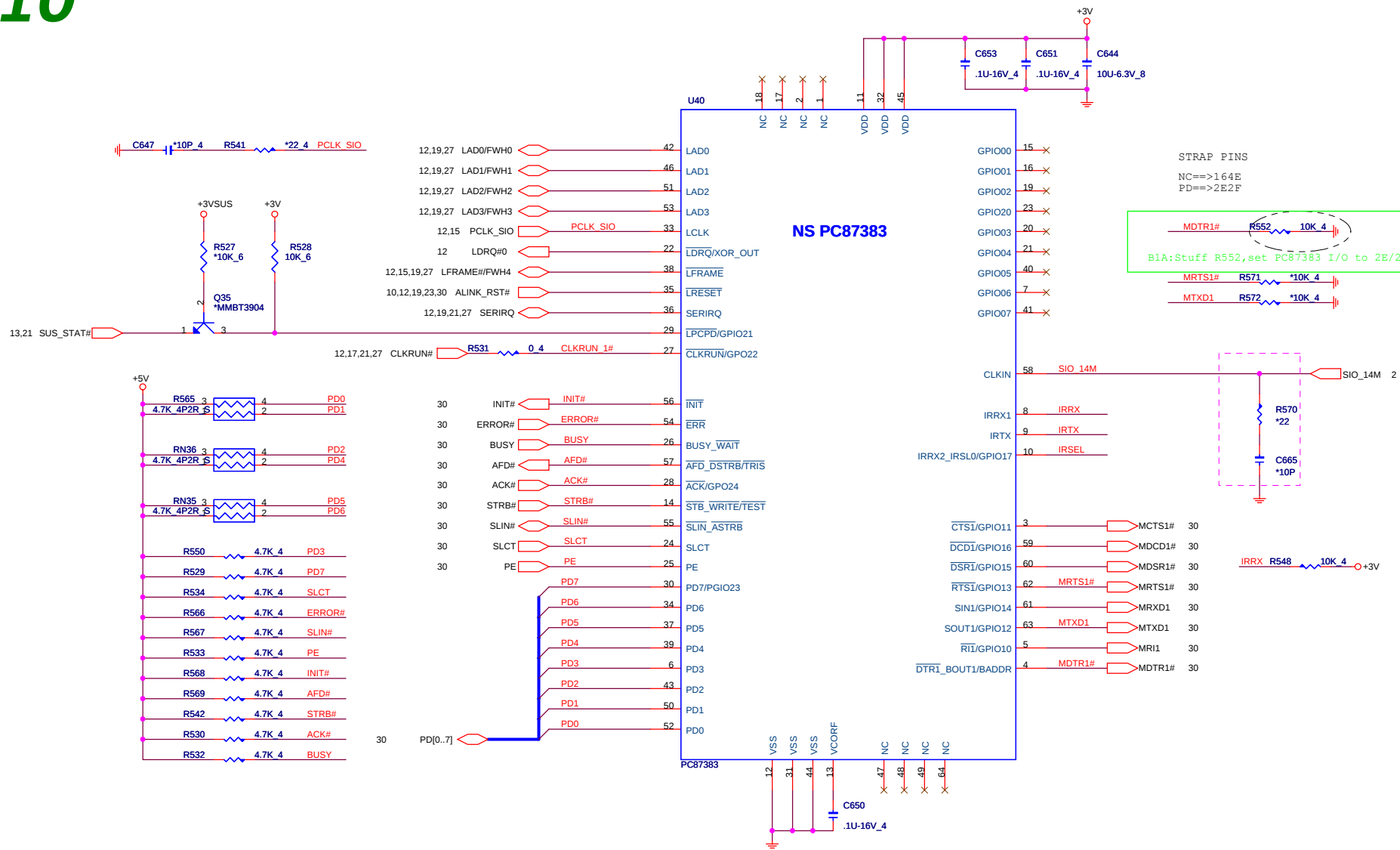


PROJECT :ZH3
Quanta Computer Inc.

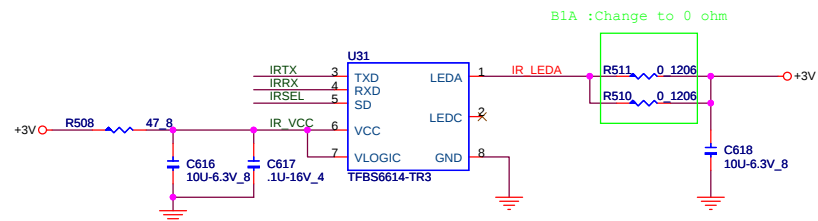
Size	Document Number	Rev
	REALTEK ALC883 & MDC & LINE OUT Amplifier	D
Date:	Tuesday, June 27, 2006	Sheet 24 of 36

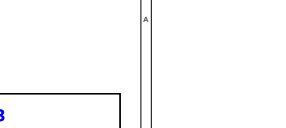
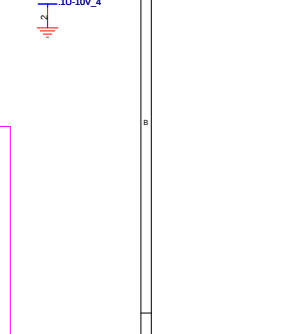
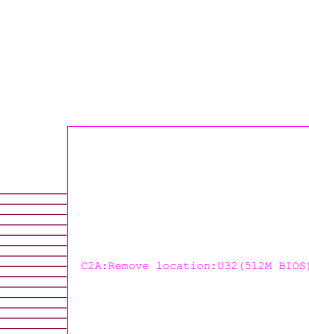
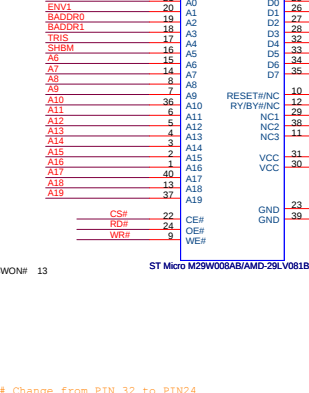
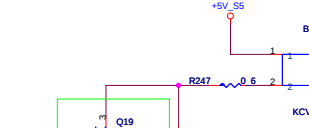
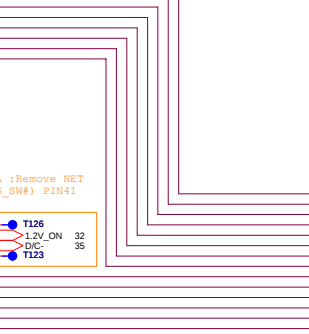
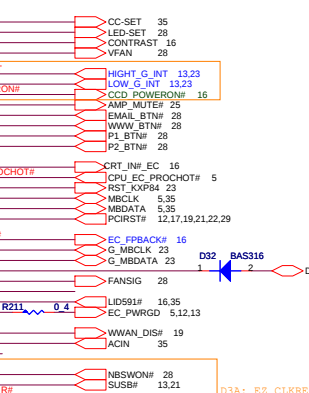
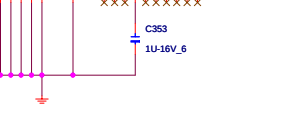
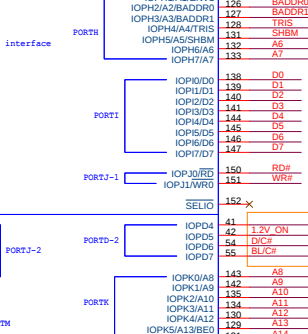
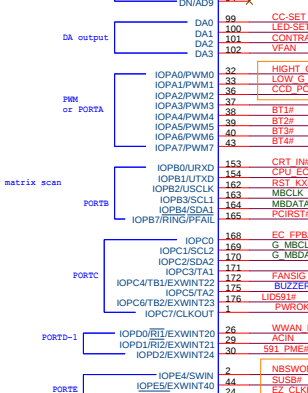
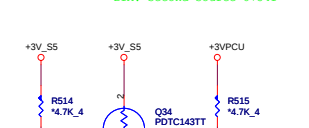
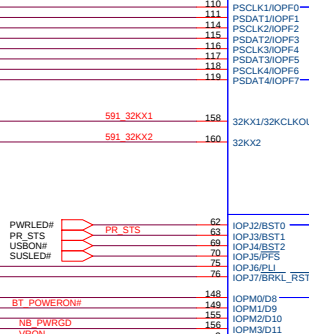
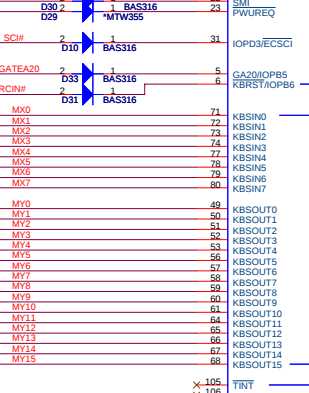
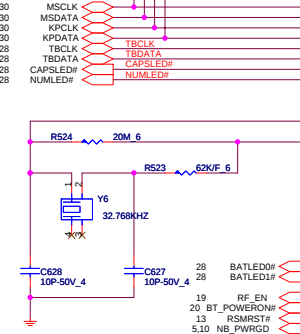
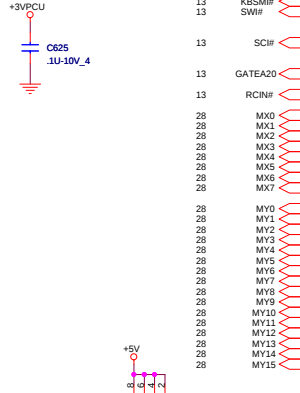
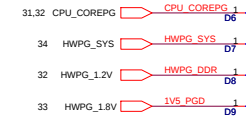
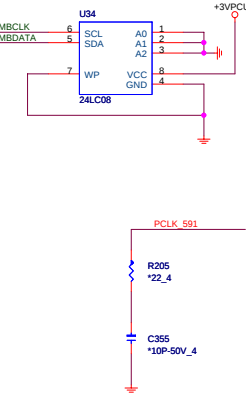
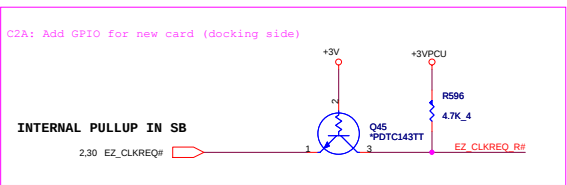


SIO



FIR

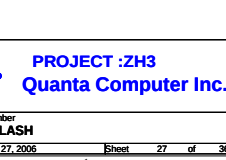
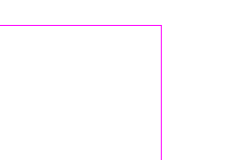
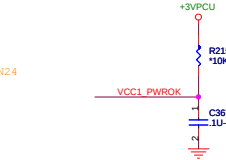
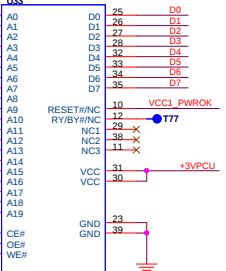




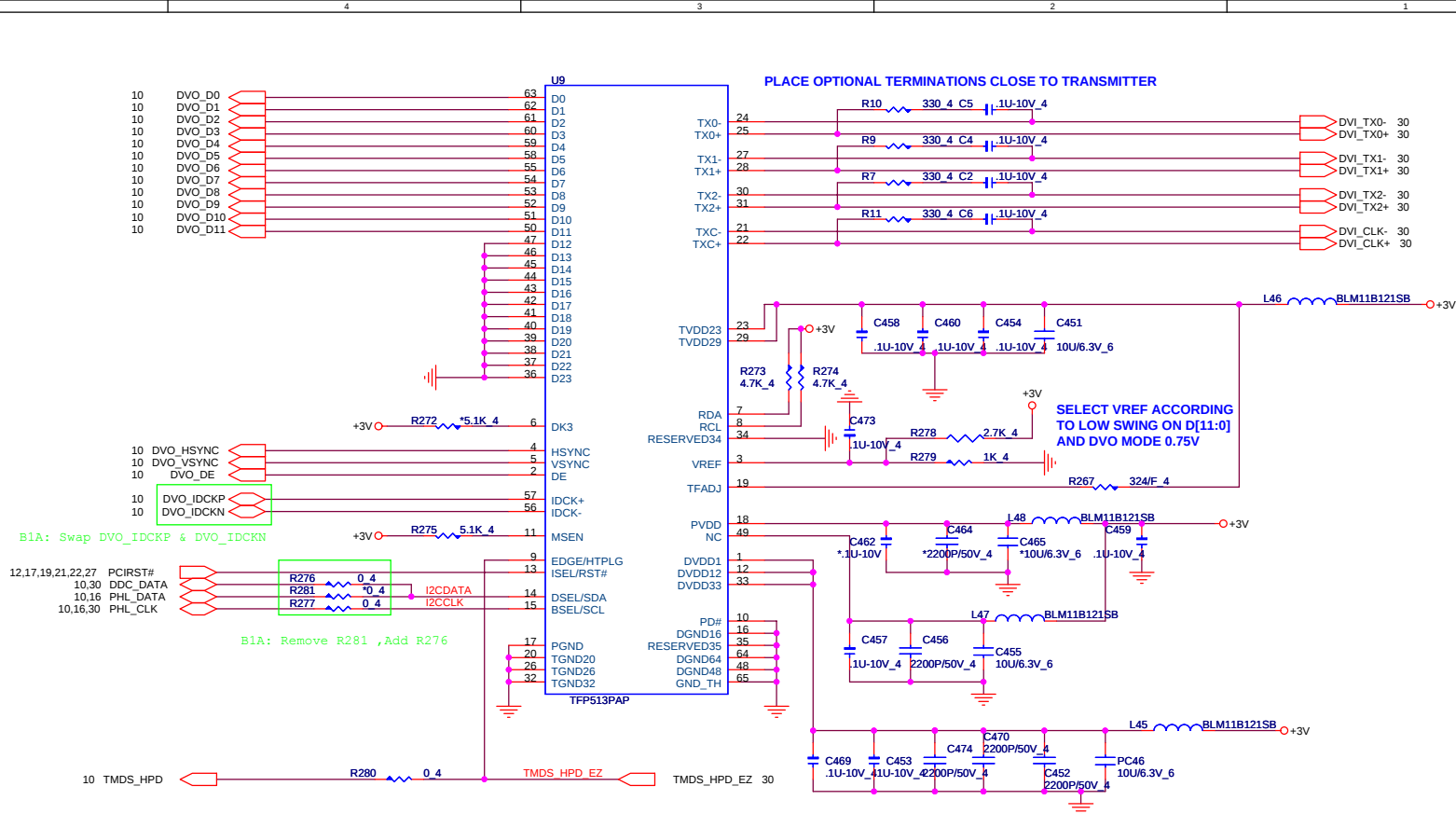
I/O Address		
BAUDR1-0	Index	Data
0 0	4E	4F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	Reserved
1 1	Reserved	

WIRELESS_SW# R512 4.7K_4

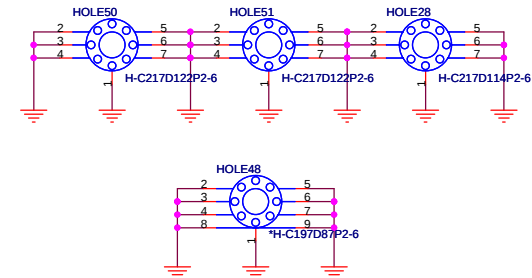
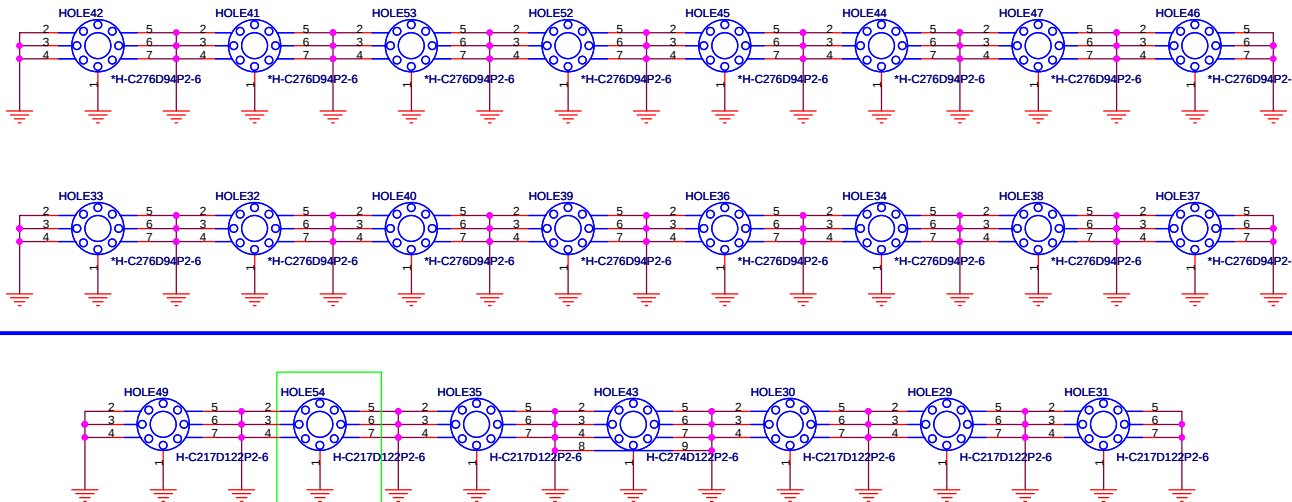
BLUETOOTH_SW# R513 4.7K_4



PROJECT :ZH3
Quanta Computer Inc.



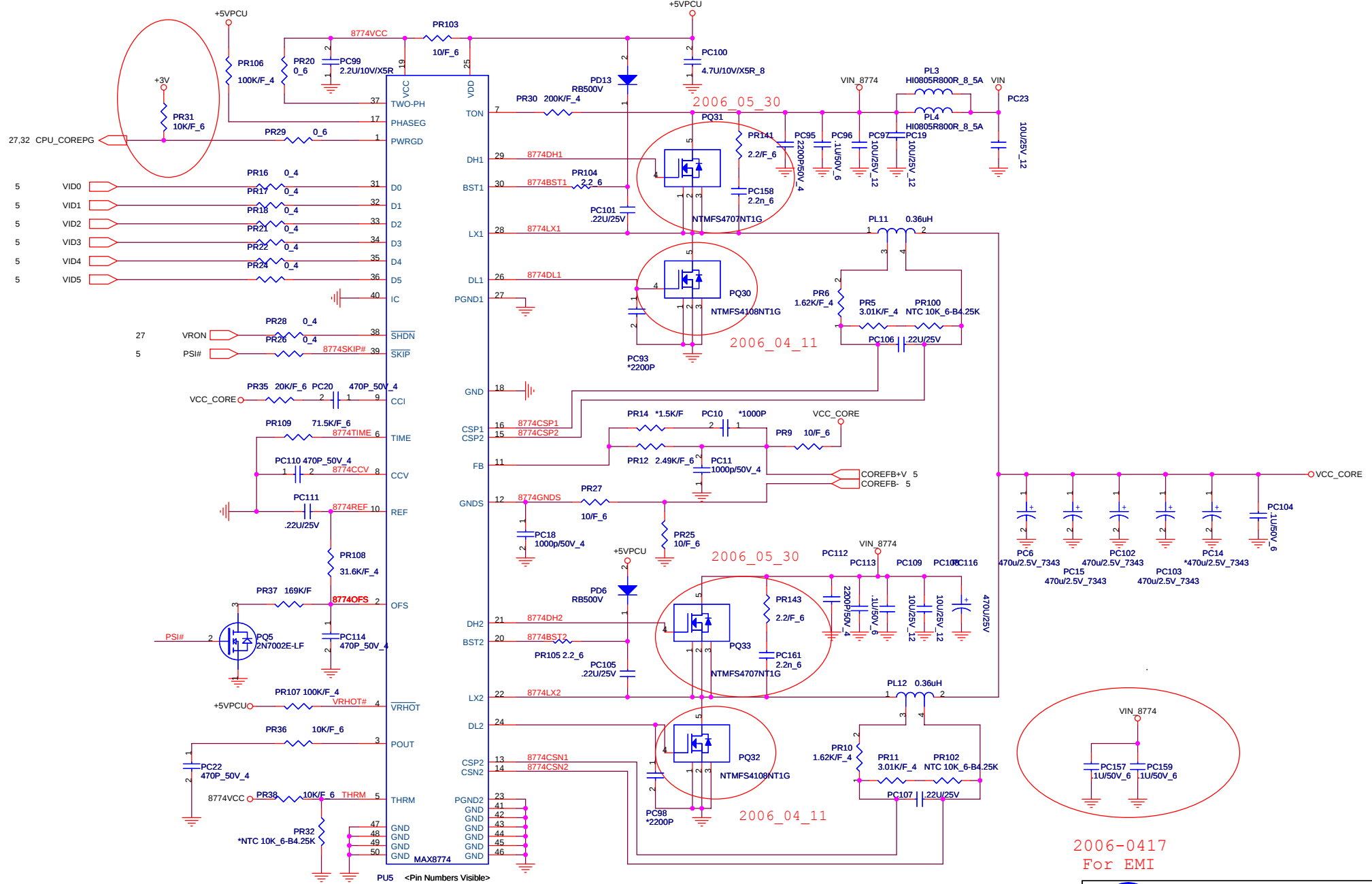
HOLE



PROJECT :ZH3
Quanta Computer Inc.

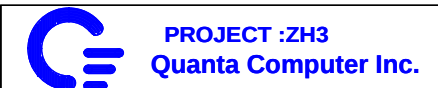
Size	Document Number	Rev
	CH7307& HOLE	D
Date:	Tuesday, June 27, 2006	Sheet 29 of 36

2006_03_06 for AMD

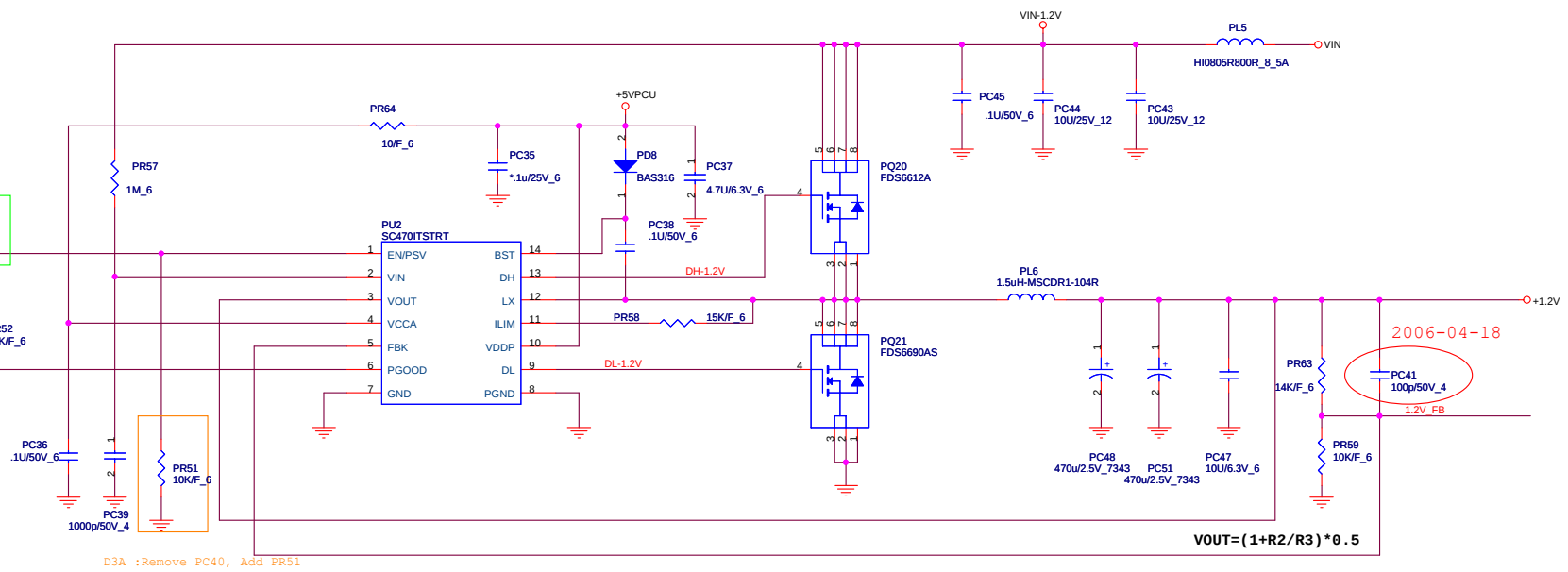
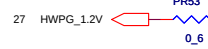
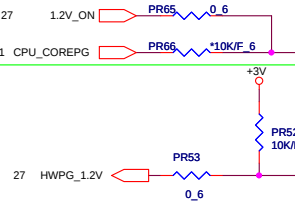


PUS <Pin Numbers Visible>
B1A:PUS Change footprint to -50P

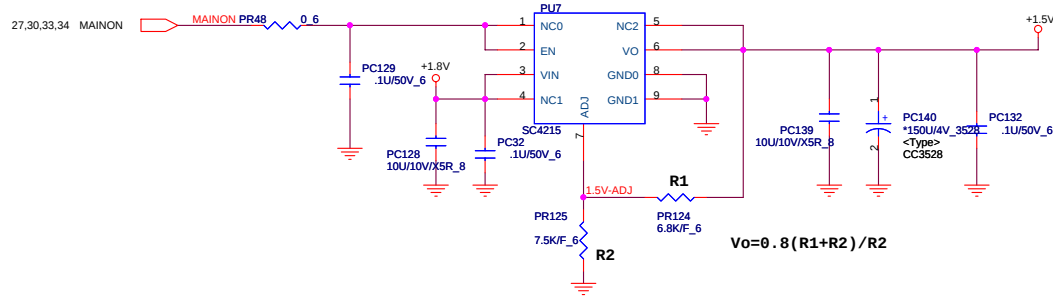
2006-0417
For EMI



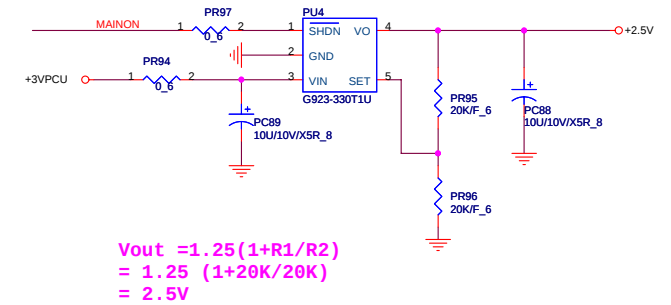
C2A :Modify to EC control ,
Remove PR66, Stuff PR65



D3A :Remove PC40, Add PR51



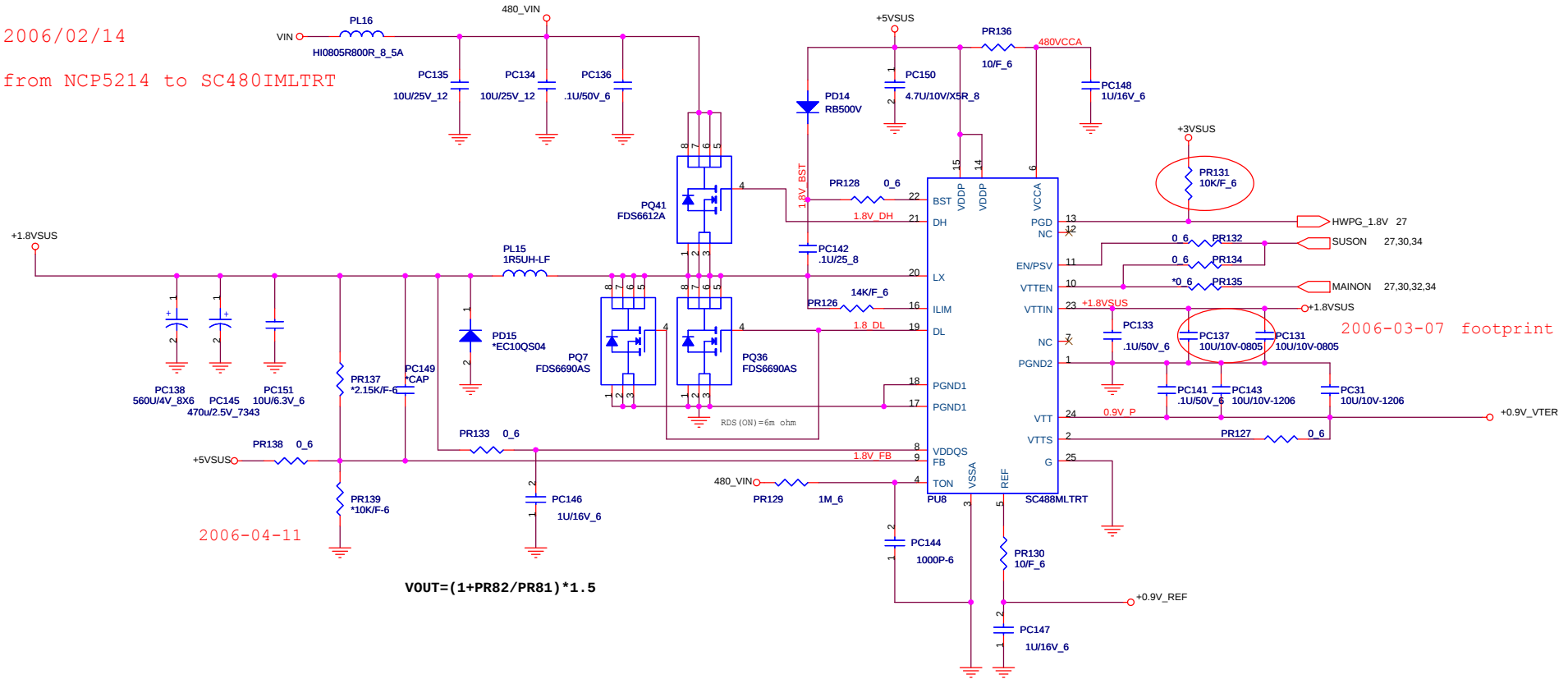
$$Vo = 0.8 \frac{(R1 + R2)}{R2}$$



$$Vout = 1.25 \left(1 + \frac{R1}{R2} \right) = 1.25 \left(1 + \frac{20K}{20K} \right) = 2.5V$$

2006/02/14

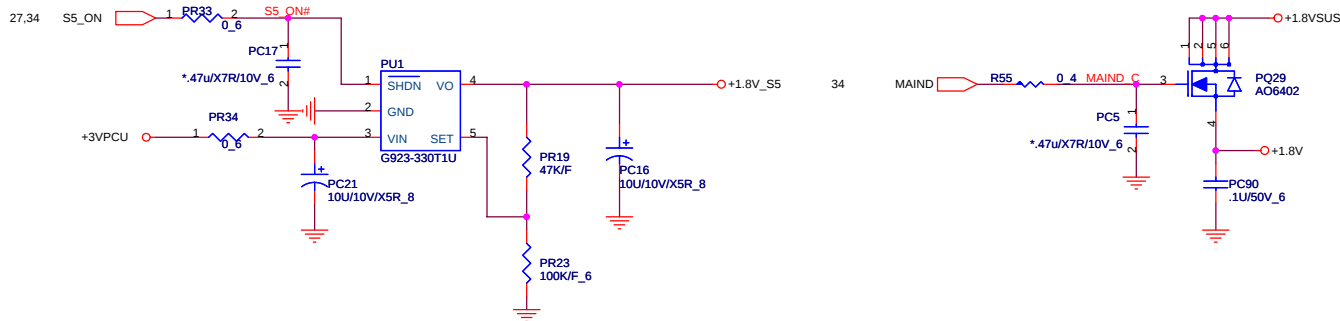
change from NCP5214 to SC480IMLTTRT



2006-04-11

$$V_{OUT} = (1 + PR82/PR81) * 1.5$$

2006-03-07 footprint



$$\begin{aligned} V_{out} &= 1.25(1 + R1/R2) \\ &= 1.25(1 + 44K/100K) \\ &= 1.8V \end{aligned}$$

Change list

Item	Fixed Issue	Modify List	Schematic Rev.	PG#	
1	New card issue.	NC_EN# connect the PIN4 & PIN17 of CN2 and PIN11 & PIN12 of CN14	B	13,31	
2	New card issue.	Change from USB8 to USB5 for new card,	B	13,31	
3	Lan issue.	Signal change from INTF to INTG	B	12,17	
4	INT MIC issue.	CN8.2 change from MIC2_INT to MIC_GND	B	25	
5	Wireless LED issue.	SW2.1 change from GND to wireless_sw#, SW2.2 change from wireless_sw# to GND.PIN3,4 is float	B	28	
6	DVI issue	Q40.1 change from PHL_DATA to DDC_DATA	B	29,30	
7	RAMP test				
8					
9					
10					
1					
2					
3					
4					
5					
6					
7					
8					
1					
2					
3					

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